This listing of claims will replace all prior versions, and listings, of claims in the application:

Listing of Claims:

Claim 1 (Previously presented): A method for interfacing a first component and a second component, the first component being associated with a first electrical interface and first communication type, and the second component being associated with a second electrical interface and second communication type, comprising the following steps:

receiving from the first component a request for an access operation comprising one of at least a write operation and a read operation, the request comprising a requested data address associated with the second component;

determining whether data corresponding to the requested data address is missing from memory, the memory being independent of the second component; and

when the data is missing from the memory, intercepting the request, loading the data from the second component to the memory, and performing the requested access operation, wherein modified data is converted from the first communication type to the second communication type and written to the memory and to the second component during a write operation, and wherein data is converted from the second communication type to the first communication type and read by the first component during a read operation.

Claim 2 (Previously presented): The method according to claim 1, wherein the step of determining whether data is missing from memory comprises determining whether the data is stored in an associated cache memory, and wherein the steps of intercepting the request and loading the data respectively comprise generating an interrupt request and writing the data to the associated cache memory, wherein the request for an access operation from the first component is detained in response to the interrupt request while the data is being written to the associated cache memory.

Claim 3 (Previously presented): The method according to claim 2, wherein the step of determining whether the data is stored in an associated cache memory comprises comparing the requested data address with addresses of data currently stored in the associated cache memory.

Claim 4 (Original): The method according to claim 2, wherein the step of writing the data to the associated cache memory comprises writing the data to a portion of the associated cache memory associated with stored data that is older than stored data associated with other portions of the associated cache memory.

Claim 5 (Original): The method according to claim 4, wherein the associated cache memory comprises cylinder random access memory and wherein the step of writing the data to a portion of the associated cache memory comprises writing the data to a page in the cylinder random access memory that is older than other pages in the cylinder random access memory.

Claim 6 (Previously presented): The method according to claim 5, wherein the step of writing the data to a page comprises the steps of:

determining which of the pages in the cylinder random access memory is oldest;

determining which tracks of data within the oldest page have been modified;

writing the tracks of data within the oldest page which have been modified to the second component;

reading the data from the second component; and

writing the data to the oldest page.

Claim 7 (Original): The method according to claim 1, wherein the first communication type comprises a serial stream format and the second communication type comprises a parallel stream format.

Claim 8 (Previously presented): The method according to claim 1, wherein during a write operation the modified data comprises a serial data stream, said method further comprising the steps of:

synchronizing a clock signal with the serial data stream;

shifting the synchronized serial data stream into a serial-to-parallel register; and

shifting a parallel data stream out of the register, wherein the serial-to-parallel register converts the serial data stream to the parallel data stream.

Claim 9 (Previously presented): The method according to claim 1, wherein during a read operation the data comprises a parallel data stream, said method further comprising:

shifting the parallel data stream into a parallel-to-serial register; and

shifting a serial data stream out of the register, wherein the parallel-to-serial register converts the parallel data stream to the serial data stream.

Claims 10-33 (Canceled).

Claim 34 (Original): The method of claim 1, wherein the step of performing the requested access operation comprises performing the access operation autonomously, whereby the access operation is performed without processor intervention.

Claim 35 (Original): A computer readable medium, comprising instructions capable of performing the method of claim 1.

Claims 36-37 (Canceled).